CLAIMS

What is claimed is:

Sub A1

1. A dual processor system, comprising:

(a) a first processor coupled to a system address bus and a data bus; and

(b) a second processor coupled to the system address bus and to the data bus, the second processor comprising a control register having a control register system address, an internal memory, a data register having a data register system address and coupled to the internal memory, and an internal address generator coupled to the control register and to the internal memory, wherein:

the control word is written into the control register when the first processor places a control word having a burst mode bit and a starting internal address on the data bus and asserts the control register system address on the system address bus; and

the second processor enters a burst mode in which the internal address generator selects consecutive memory locations of the internal memory, starting at the starting internal address specified in the control word stored in the control register, during subsequent data transfer cycles, when the control word has a burst mode bit indicating burst mode.

2. The dual processor system of claim 1, wherein the system is implemented as an integrated circuit.

3. The dual processor system of claim 1 wherein the second processor remains in the burst mode only so long as the first processor asserts the data register system address on the system address bus.

4. The dual processor system of claim 1, wherein, in a write burst mode, the first processor asserts the data register system address on the system address bus and writes subsequent data words on the data bus, and the internal address generator selects consecutive memory locations of the internal memory, starting at the starting internal address, whereby the subsequent data words are written into the consecutive memory locations.

5. The dual processor system of claim 1, wherein, in a read burst mode, the first processor asserts the data register system address on the system address bus and reads

subsequent data words on the data bus, the internal address generator selects consecutive memory locations of the internal memory, starting at the starting internal address, and the data register reads data words at the consecutive memory locations and places said data words on the data bus, whereby the subsequent data words are read from the consecutive memory locations by the first processor.

6. The dual processor system of claim 1, wherein the second processor is a co-processor.

7. The dual processor system of claim 1, wherein:

the control word is written into the control register when the first processor places a control word having a burst mode bit and a starting internal address on the data bus and asserts the control register system address on the system address bus; and

the second processor enters a single data transfer mode in which the internal address generator selects the starting internal address specified in the control word stored in the control register, during a next data transfer cycles when the control word has a burst mode bit that does not indicate burst mode.

8. The dual processor system of claim 1, wherein the first processor and second processor are intercoupled by the system address bus, the data bus, a chip select line, a read signal line, and a write signal line.

9. The dual processor system of claim 1, wherein:

the internal memory comprises a plurality of memory blocks;

the control word comprises the burst mode bit field, a memory bank field which specifies a selected memory bank of the plurality of memory banks, and an internal bank address field which specifies the starting internal bank address within the selected memory bank; and

the internal address generator determines the starting internal address from the selected memory bank and the internal bank address of the control word.

10. An integrated circuit having a second processor for transferring data with a first processor coupleable to the second processor via a system address bus and a data bus, the second processor comprising a control register having a control register system address, an

internal memory, a data register having a data register system address and coupled to the internal memory, and an internal address generator coupled to the control register and to the internal memory, wherein:

the control word is written into the control register when the first processor places a control word having a burst mode bit and a starting internal address on the data bus and asserts the control register system address on the system address bus; and

the second processor enters a burst mode in which the internal address generator selects consecutive memory locations of the internal memory, starting at the starting internal address specified in the control word stored in the control register, during subsequent data transfer cycles, when the control word has a burst mode bit indicating burst mode.

11. The integrated circuit of claim 10, wherein the second processor remains in the burst mode only so long as the first processor asserts the data register system address on the system address bus.

12. The integrated circuit of claim 10, wherein, in a write burst mode, the first processor asserts the data register system address on the system address bus and writes subsequent data words on the data bus, and the internal address generator selects consecutive memory locations of the internal memory, starting at the starting internal address, whereby the subsequent data words are written into the consecutive memory locations.

13. The integrated circuit of claim 10, wherein, in a read burst mode, the first processor asserts the data register system address on the system address bus and reads subsequent data words on the data bus, the internal address generator selects consecutive memory locations of the internal memory, starting at the starting internal address, and the data register reads data words at the consecutive memory locations and places said data words on the data bus, whereby the subsequent data words are read from the consecutive memory locations by the first processor.

14. The integrated circuit of claim 10, wherein the second processor is a co-processor.

15. The integrated circuit of claim 10, wherein the first processor and second processor are intercoupled by the system address bus, the data bus, a chip select line, a read signal line, and a write signal line.

16. The integrated circuit of claim 10, wherein:

the internal memory comprises a plurality of memory blocks;

the control word comprises the burst mode bit field, a memory bank field which specifies a selected memory bank of the plurality of memory banks, and an internal bank address field which specifies the starting internal bank address within the selected memory bank; and

the internal address generator determines the starting internal address from the selected memory bank and the internal bank address of the control word.